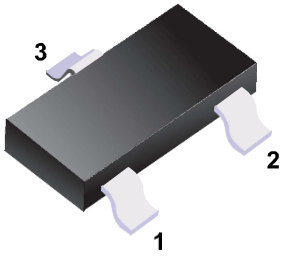
2N7002 SOT-23

MOSFET N-CHANNEL Enhancement

■ High Speed Switching Applications

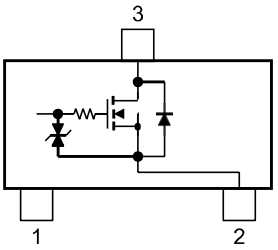
- ESD protected gate
- Low ON-resistance

$R_{DS(on)}$ = 2.8 Ω (typ.) (@V_{GS} = 10 V)
$R_{DS(on)}$ = 3.1 Ω (typ.) (@V_{GS} = 5 V)
$R_{DS(on)}$ = 3.2 Ω (typ.) (@V_{GS} = 4.5 V)



1.GATE
2.SOURCE
3.DRAIN

■ **Simplified outline(SOT-23)**



Equivalent Circuit (top view)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain–source voltage		V_{DSS}	60	V
Gate–source voltage		V_{GSS}	± 20	V
Drain current (Note1)	DC	I_D	200	mA
	Pulse	I_{DP} (Note 2)	760	
Power dissipation		P_D (Note 3)	320	mW
		P_D (Note 4)	1000	
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150°C during use.

Note 2: Pulse width ≤ 10 μs, Duty ≤ 1%

Note 3: Mounted on an FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.42 mm^2 x 3)

Note 4: Mounted on an FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

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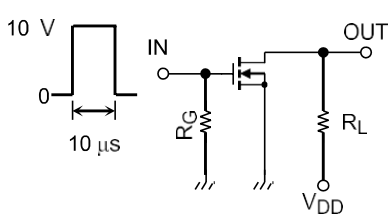
Electrical Characteristics (Ta = 25°C, Otherwise specified)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 250 μA, V_{GS} = 0 V	60	—	—	V
Drain cutoff current		I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	—	—	1	μA
			V_{DS} = 60 V, V_{GS} = 0 V, Tj=150 °C	—	—	200	
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±2	μA
			V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±0.5	
			V_{GS} = ±5 V, V_{DS} = 0 V	—	—	±0.1	
Gate threshold voltage		V_{th}	I_D = 250 μA, V_{DS} = V_{GS}	1.1	—	2.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 200 mA (Note 5)	—	450	—	mS
Drain-source ON-resistance		$R_{DS(ON)}$ (Note 5)	I_D = 100 mA, V_{GS} = 10 V	—	2.8	3.9	Ω
			I_D = 100 mA, V_{GS} = 10 V, Tj=150 °C	—	5.4	8.1	
			I_D = 100 mA, V_{GS} = 5 V	—	3.1	4.4	
			I_D = 100 mA, V_{GS} = 4.5 V	—	3.2	4.7	
Total Gate Charge		$Q_{G(tot)}$	V_{DS} = 30 V, I_D = 200 mA, V_{GS} = 4.5 V	—	0.27	0.35	nC
Gate-Source Charge		Q_{GS}		—	0.08	—	
Gate-Drain Charge		Q_{GD}		—	0.08	—	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	11	17	pF
Output capacitance		C_{oss}		—	3	—	
Reverse transfer capacitance		C_{rss}		—	0.7	—	
Switching time	Turn-on delay time	$t_{d(on)}$	V_{DD} = 40 V, I_D = 160 mA, V_{GS} = 0 V to 10 V, R_G = 50 Ω	—	2	4	ns
	Rise time	t_r		—	3	—	
	Turn-off delay time	$t_{d(off)}$		—	7	14	
	Fall time	t_f		—	24	—	
Drain-source forward voltage		V_{DSF}	I_D = -115 mA, V_{GS} = 0 V (Note 5)	—	-0.87	-1.2	V

Note 5: Pulse test

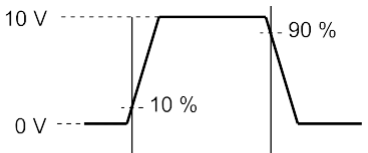
Switching Time Test Circuit

(a) Test Circuit

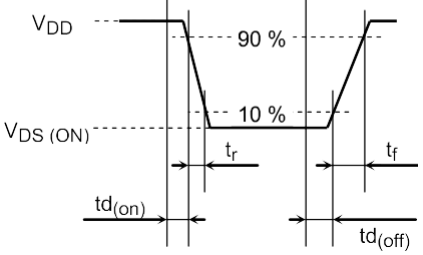


V_{DD} = 40 V
R_G = 50 Ω
D.U. ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

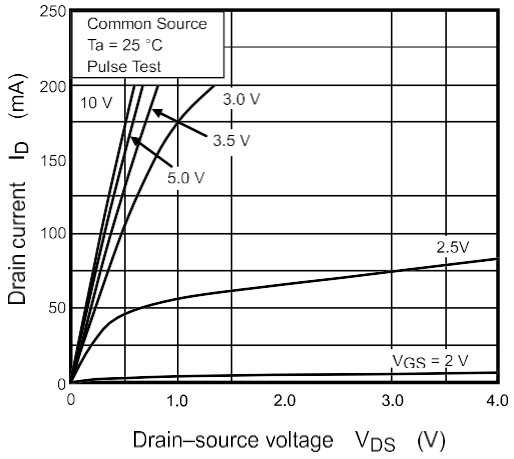
(b) V_{IN}



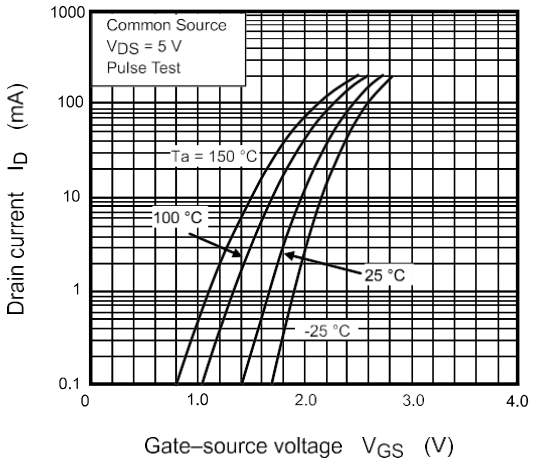
(c) V_{OUT}



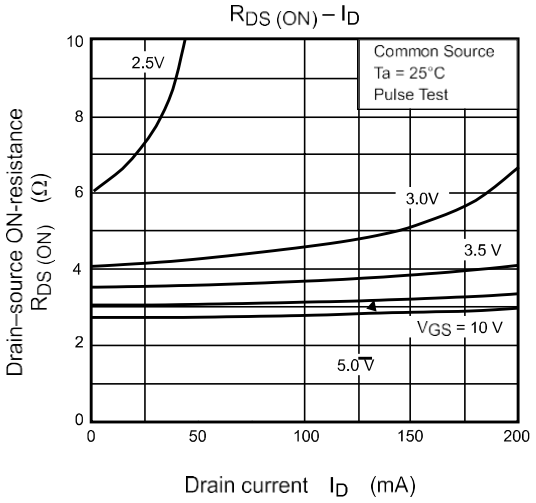
$I_D - V_{DS}$



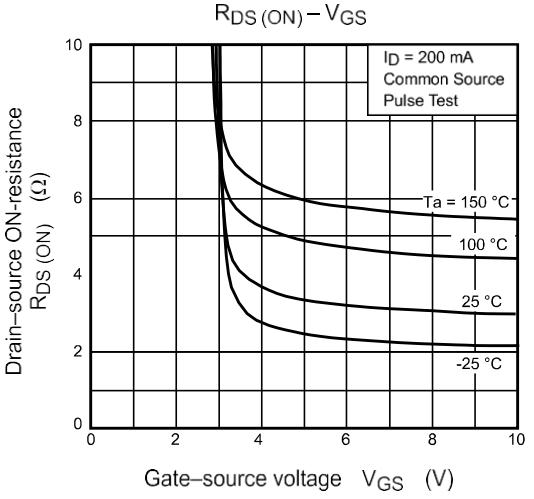
$I_D - V_{GS}$



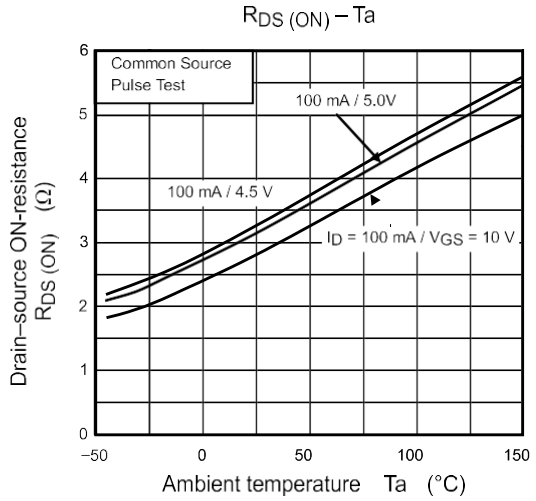
$R_{DS\ (ON)} - I_D$



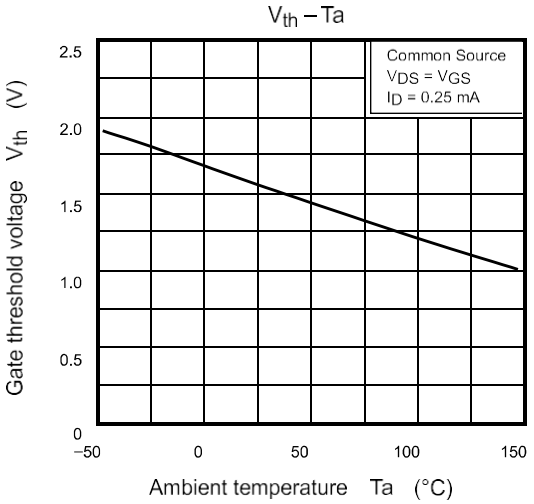
$R_{DS\ (ON)} - V_{GS}$



$R_{DS\ (ON)} - Ta$



$V_{th} - Ta$



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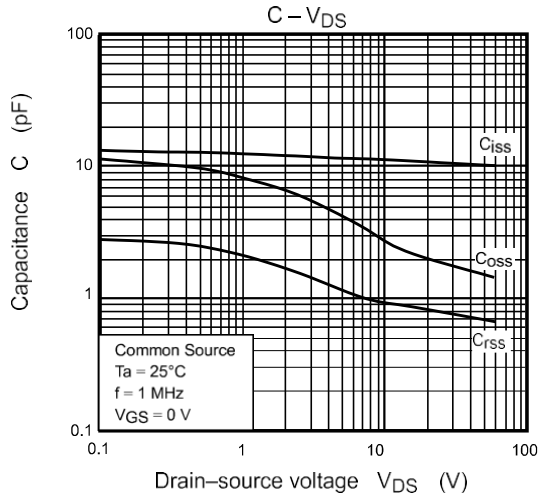

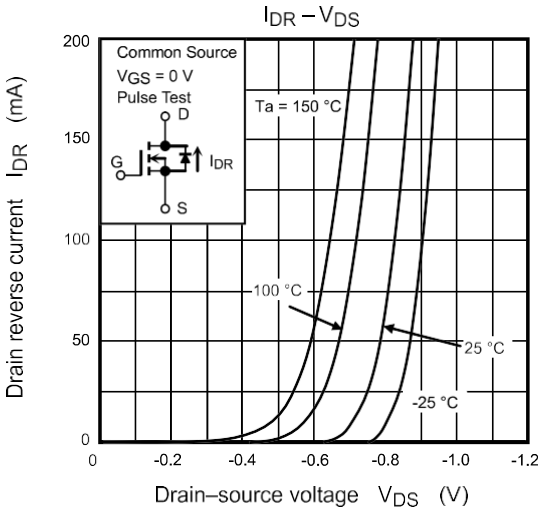

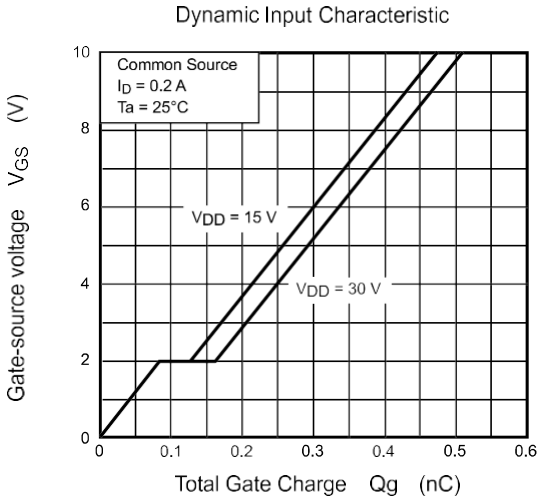

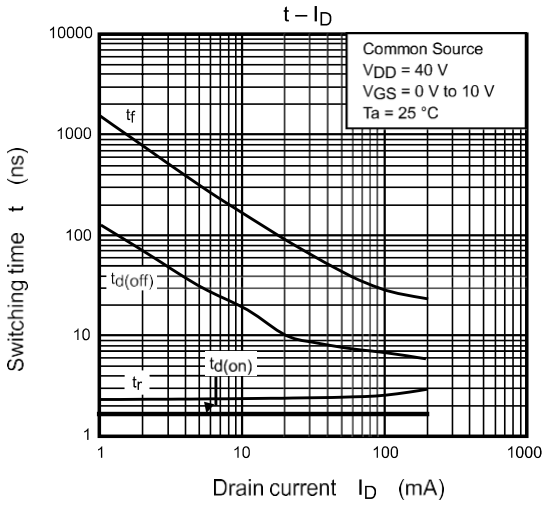

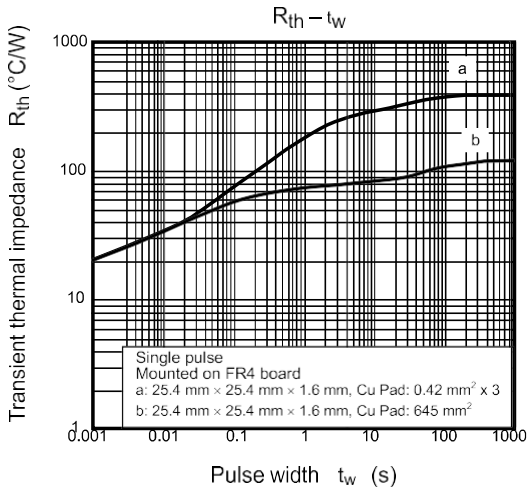

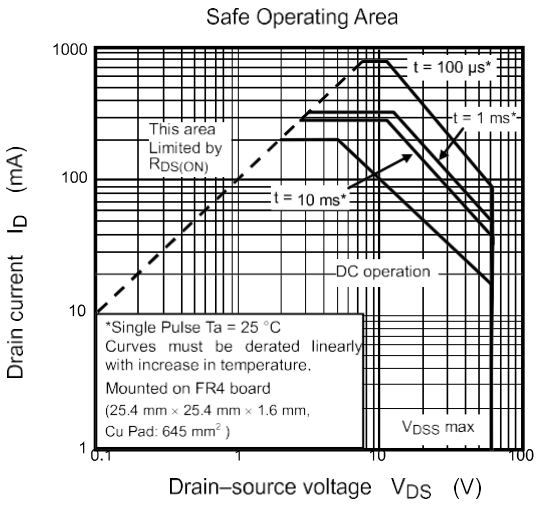

Note: The above characteristics curves are presented for reference only and not guaranteed by production test.

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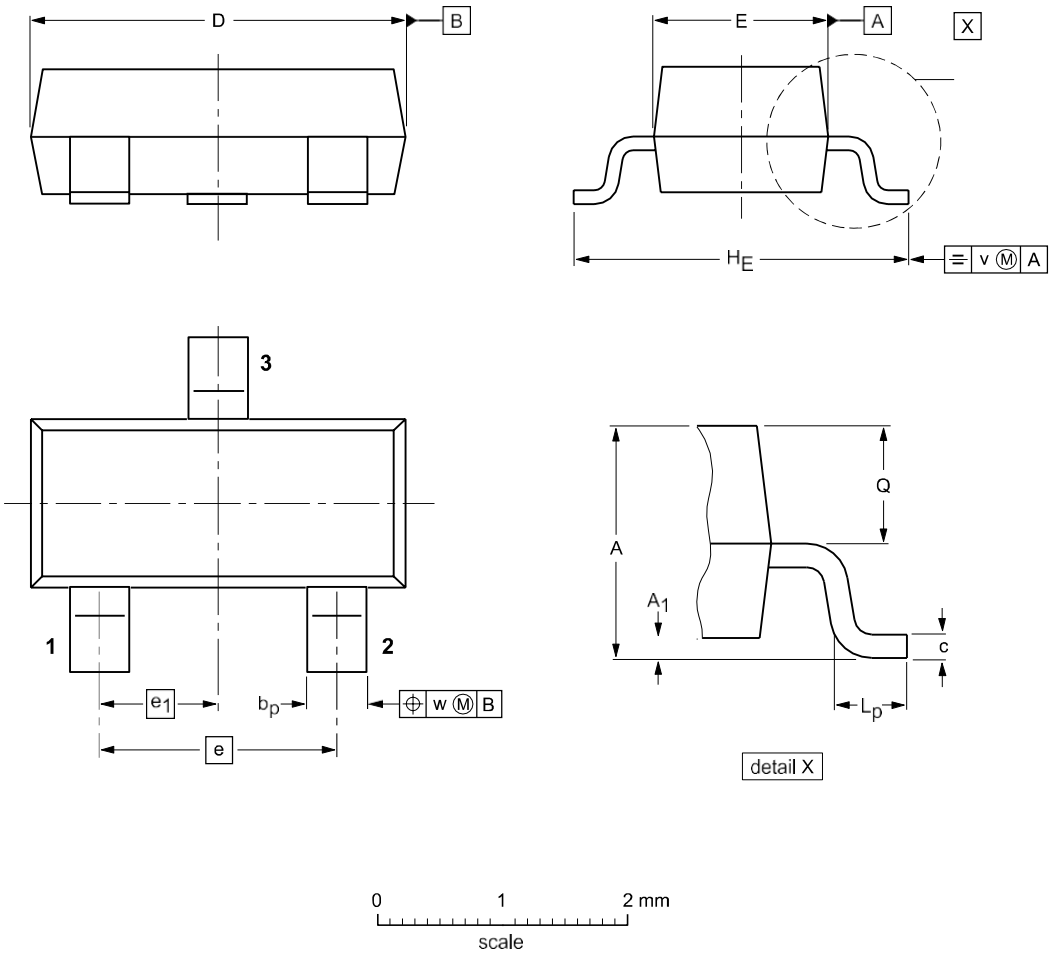

DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

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